CLAIMS

What is claimed is:

1. A base station controller for a wireless network, comprising:

a plurality of processor boards, each processor board having a local timer; and

a plurality of timing units, each timing unit generating timing cells, each timing cell containing time information, and each timing unit transmitting timing cells to each one of the plurality of processor boards;

wherein a processor board realigns its local timer with time information contained in a received timing cell whenever its local timer drifts from the time information contained in the received timing cell by a predetermined time offset.

2. The base station controller of claim 1, wherein the predetermined time offset is approximately 1 ms.

3. The base station controller of claim 1, wherein each processor board alternately receives a timing cell from each one of the timing units.

4. The base station controller of claim 1, wherein the timing cells are transmitted to the processor boards over an Asynchronous Transfer Mode (ATM) network.

5. The base station controller of claim 1, wherein the timing cells are transmitted to the processor boards over an Ethernet network.

6. The base station controller of claim 1, wherein the timing cells are transmitted to the processor boards over a universal serial bus.

7. The base station controller of claim 1, wherein a processor board does not realign its local timer with time information contained in a received timing cell when a time difference between its local timer and the time information contained in the received timing cell exceeds an error threshold, the error threshold being greater than the time offset.

8. The base station controller of claim 7, wherein the error threshold is approximately 2 ms.

9. The base station controller of claim 3, wherein at least one of the processor boards stores a fault status flag in a local memory, the fault status flag indicating a timing condition of the respective processor board.

10. The base station controller of claim 9, wherein the fault status flag indicates an inoperable timing condition of the respective processor board when time differences between the respective local timer and time information contained in a received timing cell from each one of the timing units exceed a predetermined error threshold.

11. The base station controller of claim 10, further comprising:

a main processor having a local database for periodically retrieving the fault status flag from the processor boards and storing the retrieved fault status flag in the local database; and

a resource manager for assigning incoming calls to the processor boards based on the retrieved fault status flag.

12. The base controller of claim 11, wherein the resource manager does not assign incoming calls to a processor board when the retrieved fault status flag of the processor board indicates an inoperable timing condition.

13. A method for distributing timing information to the processor boards in a base station controller comprising a plurality of processor boards, each processor board having a local timer, and a plurality of timing units, comprising the steps of:

generating timing cells from each one of the timing units, each timing cell containing time information;

transmitting timing cells from each one of the timing units to each one of the processor the processor boards; and

realigning the local timer of a processor board with time information contained in a received timing cell when its local timer drifts from the time information contained in the received timing cell by a predetermined time offset.

14. The method of claim 13, wherein the predetermined time offset is approximately 1 ms.

15. The method of claim 13 further comprising the step of alternately receiving a timing cell at a processor board from each one of the timing units.

16. The method of claim 13, further comprising the step of transmitting the timing cells to the processor boards over an Asynchronous Transfer Mode (ATM) network.

17. The method of claim 13, further comprising the step of transmitting the timing cells to the processor boards over an Ethernet network.

18. The method of claim 13, further comprising the step of transmitting the timing cells to the processor boards over a Universal Serial Bus.

19. The method of claim 13, further comprising the steps of not realigning the local timer of a processor board with time information contained in a received timing cell when a time difference between the local timer of the processor board and the received time information exceeds a predetermined error threshold, the error threshold being greater than the time offset.

20. The method of claim 19, wherein the predetermined error threshold is approximately 2 ms.

21. A transceiver comprising:

a plurality of processor boards; and

a timing network containing a plurality of timing units, each timing unit continuously providing a timing signal to each of the plurality of processor boards for setting a standard time.

22. The transceiver of claim 21, wherein each of the plurality of timing units provides its respective timing signal at a different time so as to alternate the continuous timing signals from each timing unit.

23. The transceiver of claim 22, wherein the timing signals are generated from a GPS timing reference and are used to adjust a local timer in each one of the plurality of processor boards to the standard time.

24. A wireless communication system, comprising:

a mobile station (MS); and

a base station (BS) in communication with the MS, the BS comprising:

a plurality of processor boards; and

a timing network containing a plurality of timing units, each timing unit continuously providing a timing signal to each of the plurality of processor boards for setting a standard time.

25. The system of claim 24, wherein each of the plurality of timing units provides its respective timing signal at a different time so as to alternate the continuous timing signals from each timing unit.

26. The system of claim 25, wherein the timing signals are generated from GPS timing reference and are used to adjust a local timer in each one of the plurality of processor boards to the standard time.